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68605 (6653)

Amendments to the Claims:

1 (currently amended): A method of power sequence protection for a level shifter comprising the steps of:

(a) placing the level shifter in a pre-selected state if an input voltage supply for an input signal is not powered on before an output voltage supply for an output signal is powered on; and

(b) releasing the level shifter from the pre-selected state to follow transitions of an input signal when the input voltage supply and the output voltage supply are [[is]] powered on.

2 (original): The method of Claim 1 wherein step (a) comprises connecting a common voltage rail to an output signal port or an inverted output signal port of the level shifter.

3 (original): The method of Claim 2 wherein step (b) comprises presenting a high impedance to the output signal port or the inverted output signal port of the level shifter.

4 (currently amended): A power sequence protection circuit comprising:

a latch electrically coupled to an input voltage supply and an output voltage supply; and

a switch electrically coupled to the latch wherein the latch sets the switch to [[has]] a first state for holding a level shifter in a pre-selected state if the output voltage supply is powered on when the input voltage supply is not powered on and wherein the latch sets the switch to a second state for releasing the level shifter from the pre-selected

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state when to follow transitions of an input signal if the input voltage supply and the output voltage supply are [[is]] powered on.

5 (original) : The power sequence protection circuit of Claim 4 wherein the switch connects a common voltage rail to an output signal port or an inverted output signal port of the level shifter in the first state.

6 (original) : The power sequence protection circuit of Claim 5 wherein the switch presents a high impedance to the output signal port or the inverted output signal port of the level shifter in the second state.

7 (original) : The power sequence protection circuit of Claim 4 further comprising the level shifter.

8 (previously presented) : A power sequence protection circuit comprising:

a switch connected to a level shifter between an output signal port or an inverted output signal port of the level shifter and a common voltage rail; and

a latch connected to the switch to drive the switch to a conducting state if an input voltage supply is not powered on when an output voltage supply is powered on and to drive the switch to a non-conducting state if the input voltage supply and is powered on when the output voltage supply are [[is]] powered on.

9 (previously presented) : The power sequence protection circuit of Claim 8 wherein the switch comprises two field effect transistors connected in series.

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10 (previously presented): The power sequence protection circuit of Claim 8 wherein the latch comprises two field effect transistors connected in series between a third field effect transistor and the common voltage rail.